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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,409	03/26/2004	Kuo-Chi Tu	TSM03-0731	3277

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SLATER & MATSIL, L.L.P.
17950 PRESTON ROAD, SUITE 1000
DALLAS, TX 75252

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,409	TU ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-57 is/are pending in the application.

4a) Of the above claim(s) 1-25, 33-35, 43-57 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 26-32 and 36-43 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 03/26/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 26-32 and 36-43 in the reply filed on 08/17/05 is acknowledged.

DETAILED ACTION

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 26, 27, 28, 29, 30, 31, and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US publication 2004/0084709).

With respect to claim 26, Kim et al. teach a method for forming a semiconductor device, the method comprising (see figs. 10 and associated text) :

providing a substrate 2;

forming a first interlayer dielectric 20 on the substrate;

forming connection node (the conductive 26 on the most left of figure 1);

forming a second interlayer dielectric 28 on the first interlayer dielectric;

forming an integrated capacitor (the 30,32,34 (36)) on the most left of figure 1) having a first top electrode 30 and a first bottom electrode 34 formed in the second interlayer dielectric such that the first bottom electrode is electrical contact with the connection node; and

forming a connection node contact 46b through the second interlayer dielectric providing an electrical connection to the connection node (since the source and drain are electrically connected through the channel).

With respect to claims 27 and 28, Kim et al. further teach forming a MOS device o a second region of the substrate before forming the first interlayer dielectric. See fig. 1 and associated text.

With respect to claim 29, Kim et al. further teach simultaneously forming a contact 26a in the first interlayer dielectric and the connection node, wherein the contact is electrically connected to the MOS device.

With respect to claim 30, Kim et al. further teach simultaneously forming a storage capacitor (the capacitor 36 in the right of figure 1) and the integrated capacitor (the capacitor in the left of figure 1), wherein the storage capacitor has a second top electrode 30 and a second bottom electrode 34 and the second bottom electrode is in electrical contact with the transistor via contact 26a.

With respect to claims 31 and 32, Kim et al. further teach that the connection node and the contact are formed of a first material of tungsten or metal.

4. Claims 36, 37, 38, 39, 40, 41, and 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US publication 2004/0084709).

With respect to claim 26, Kim et al. teach a method for forming a semiconductor device, the method comprising (see figs. 10 and associated text):

providing a substrate 2 having at least one first region and one second region;

forming a transistor on the first region;

forming a first interlayer dielectric 20 over the substrate;

forming connection node (the conductive 26 on the most left of figure 1) in the first interlayer dielectric upon the second region, the connection node being a thickness substantially equivalent to the thickness of the first interlayer dielectric ;

forming a second interlayer dielectric 28 on the first interlayer dielectric;

forming an integrated capacitor (the 30,32,34 (36)) on the most left of figure 1) in the second interlayer dielectric upon the second region and a storage capacitor (the capacitor 36 in the right of figure 1) in the second interlayer dielectric upon the first region, the integrated capacitor having a first bottom electrode 34 being in electrical contact with the connection node and the storage capacitor having a second bottom electrode 34, the second bottom electrode being in contact with the transistor; and

forming a connection node contact 46b in the second interlayer dielectric, the connection node contact being in electrical with the connection node (since the source and drain are electrically connected through the channel).

With respect to claim 37, Kim et al. further teach simultaneously forming a transistor contact 26a in the first interlayer dielectric and the connection node, wherein hte transistor contact connects to a source/drain of the transistor with the second bottom electrode. See figs. 10 and associated text.

With respect to claims 38, 39, and 40, Kim et al. further teach that the connection node and the contact are formed of a first material of tungsten or metal.

With respect to claims 41 and 43, Kim et al. further teach forming the connection node includes forming a barrier layer 22 on the first interlayer dielectric and forming a conductive layer of tungsten on the barrier layer.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US publication 2004/0084709).

With respect to claim 42, Kim et al. fail to teach the barrier layer is made of titanium or titanium nitride.

However, the use of titanium or titanium nitride as barrier material is well-known in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP